IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 10/423,127, filed April 25, 2003, ~~pending,~~ now U.S. Patent 6,808,947, issued October 26, 2004, which is a continuation of application Serial No. 09/934,620, filed August 22, 2001, now U.S. Patent 6,555,400, issued April 29, 2003.

Please amend paragraph number **[0003]** as follows:

[0003] State of the Art: In the fabrication of semiconductor die packages, semiconductor dice (also known as "semiconductor devices" or "semiconductor chips") are typically mounted and electrically connected to carrier substrates appropriate for the chip type and the subsequent use of the package. For example, chip-on-board (COB), board-on-chip (BOC), ball grid array (BGA), chip-scale, or leads-over-chip (LOC) mounting arrangements may be made on printed circuit board strips, tape frames and other carrier substrates known in the art. After die attach (the mounting of the semiconductor die to the carrier substrate), the hybrid combination of components is electrically connected, generally through wire bonding, conductive adhesives or solder reflow and encapsulated for protection. The finished package is then made available for use in a wide variety of applications.

Please amend paragraph number **[0004]** as follows:

[0004] Semiconductor dice and carrier substrates are distinct components which are manufactured by separate processes. Individual integrated circuit dice are usually formed from a larger structure known as a semiconductor wafer, which is typically comprised primarily of silicon, although other materials such as gallium arsenide and indium phosphide are also sometimes used. Each semiconductor wafer has a plurality of integrated circuit semiconductor dice and/or circuitry, arranged in rows and columns with the periphery of each integrated circuit being substantially rectangular in shape, the integrated circuits of the semiconductor dice being formed through a combination of deposition, etching, and photolithographic techniques. The

inactive silicon ~~backsides~~ back sides of the wafers are typically thinned (i.e., have their ~~cross sections~~ cross-sections reduced) by a mechanical and/or chemical grinding process, and the wafers sawed or "diced" into substantially rectangularly shaped discrete integrated circuit semiconductor dice. The nature and complexity of the process for fabricating integrated circuits make the manufacturing cost of an individual semiconductor die relatively high.

Please amend paragraph number **[0008]** as follows:

[0008] Referring again to drawing FIG. 1, carrier substrate 10 also includes a layer of solder resist 26. The layer of solder resist 26 is applied using photolithographic processes onto carrier substrate 10 and serves to mask or shield conductive members on the top and bottom carrier substrate surfaces during subsequent soldering and/or plating processes and/or various other processes. Various solder resist materials are well known and commercially available for such processes. With respect to the surface of carrier substrate 10, layer of solder resist ~~layer~~ 26 may mask all portions of the surface except the semiconductor die sites 20 and the contact pads for placement of solder balls 32. As previously described, pin one indicator 22 and fiducial marks 24 are typically formed as openings in the layer of solder resist ~~layer~~ 26 subsequent to the deposition thereof. Any conductive elements within semiconductor die site 20 thus remain exposed, as does at least a portion of the contact pads, after application of the layer of solder resist ~~layer~~ 26 to the top surface of the carrier substrate 10.

Please amend paragraph number **[0022]** as follows:

[0022] However, unoccupied die attach sites present several problems, namely problems relating to the structural integrity of the carrier substrate and the finished semiconductor die package. With respect to structural integrity, the carrier substrates are designed and formed with the intention of carrying a semiconductor die attached to each of the multiple die attach sites on the carrier substrate. Such attachment of the semiconductor dice provides strength to the carrier substrate in order to handle the processes associated with fabricating the semiconductor die package. Without each of the die attach sites having a die

attached thereto, the structural integrity and mechanical reliability of the carrier substrate is compromised. This problem is only exacerbated with the ongoing advances of semiconductor technology, resulting in the miniaturization of semiconductor components, which includes carrier substrates having thinner size specifications.

Please amend paragraph number **[0025]** as follows:

[0025] In operation, a heated pellet of resin mold compound 130 is disposed beneath ram or plunger 132 in pot 134. The plunger descends, melting the pellet and forcing the melted encapsulant down through sprue 136 and into primary runner 138, from which it travels to transversely oriented secondary runners 140 and across gates 142 into and through the mold cavities 144 through the short side thereof flowing across the carrier substrate 10, wherein carrier substrate 10 comprises ~~dice~~ dice 52 attached thereto, such as an array of six dice attached to a carrier substrate for positioning in and across six mold cavities 144 shown in drawing FIG. 3. Air in the runners 138 and 140 and mold cavities 144 is vented to the atmosphere through vents 146 and 148. With this arrangement, since the pellets of resin are substantially consistent in size, the melted pellets or encapsulation material thereby includes a substantially consistent volume, resulting in the shortage of encapsulation material for the transfer molding operation when having unoccupied die attach sites. Such encapsulation shortage as illustrated in drawing FIG. 3 results in defective packaging of dice.

Please amend paragraph number **[0026]** as follows:

[0026] Accordingly, what is needed in the art is a method and apparatus ~~of~~ for maintaining the structural integrity of the carrier substrate and preventing defects in the encapsulant mold and the waste thereof that are automated, accurate, low cost, relatively simple, and include high throughput.

Please amend paragraph number **[0028]** as follows:

[0028] The present invention includes a mounting substrate assembly having a substrate with a plurality of semiconductor die sites, each of the semiconductor die sites being pretested and categorized as either a good die site or a defective die site. The mounting substrate assembly may include any chip and board-type substrate or any lead frame-type assembly, either having one or more semiconductor ~~die~~ dice mounted thereon in any fashion having any type of connection with the substrate. The mounting substrate assembly includes a plurality of semiconductor dice attached to the semiconductor die sites. Each of the dice are pretested and categorized as either a good semiconductor die or a defective semiconductor die so that each good semiconductor die is attached to a good die site and each defective die is attached to a defective die site. Each of the semiconductor dice on the mounting substrate assembly is then encapsulated with an encapsulation mold in a transfer molding operation, after which the mounting substrate assembly is segregated into individual semiconductor die packages, wherein the packages are separated between the categorized good dice attached to the good die sites and defective dice attached to the defective die sites.

Please amend paragraph number **[0031]** as follows:

[0031] In another aspect of the present invention, there is a system for fabricating semiconductor die packages at various semiconductor packaging stations which may be coupled to and update the mapped information in the electronic file. Such semiconductor packaging stations include a substrate testing station, a die attach station, a molding station and a segregation station.

Please amend paragraph number **[0044]** as follows:

[0044] As illustrated in drawing FIG. 4, a block diagram depicts several stations for preparing and fabricating semiconductor die packages from a mounting substrate 200 having a plurality of dice attached thereon. In particular, the block diagram depicts the mounting substrate 200 in various fabrication processes including a substrate testing station 210, a die

attach station 230, a molding station 260 and a segregation station 270. Information regarding the mounting substrate 200 and/or the dice attached thereon is uploadable and downloadable to and from an electronic file 220 with respect to the processes undergone in the substrate testing station 210, the die attach station 230, and the segregation station 270. The mounting substrate 200 may be any suitable type mounting substrate having one or more semiconductor ~~die~~ dice mounted thereon or may be any suitable type lead frame having one or more semiconductor ~~die~~ dice mounted thereon. Also, the electrical interconnection between circuits of the substrate or leads of the lead frame may be of any suitable type, such as wire bonds, flip-chip type, etc.

Please amend paragraph number **[0049]** as follows:

[0049] As can be seen by drawing FIG. 6, lead frames may be manufactured as lead frame arrays 200′, the lead frame arrays 200′ having dimensions wide enough to accommodate a various number of semiconductor dice across a lead frame width. As illustrated in drawing FIG. 6, an exemplary lead frame array 200′ is provided with a designator 340′ located thereon. Lead frame array 200′ includes an array of semiconductor die supporting pads (die paddles) 420 and a plurality of lead fingers 422 surrounding each die paddle 420. Each lead finger 422 has, in turn, a terminal bonding portion 424 near the die paddle 420 on which the semiconductor die is to be located and an external lead 426 for connection to external circuitry on a circuit board (not shown). Tie bars 428 are provided for support of die paddle 420, and a pair of parallel side rails 470 support tie bars 428. Lead frame array 200′ may also include a pin one indicator 430 used for orientation by the vision system of automated die attach apparatus when mounting a semiconductor die to the die paddle 420. Functionally, the lead frame array 200′ can be divided into a package area 450, which includes a semiconductor die bonding area 460 therein as well as portions of lead fingers 422. The semiconductor die bonding area 460 includes die paddle 420 and the free end of the terminal bonding portions 424 of lead fingers 422. In this arrangement, designator 340′ is located in an otherwise unused peripheral surface area portion of lead frame array 200′. As one example, designator 340′ may be located on, or in close proximity to, a frame portion of lead frame array 200′, such as an unused portion of side rails 470.

Please amend paragraph number **[0050]** as follows:

[0050] Referring again to drawing FIG. 4, the mounting substrate 200 previously discussed with respect to drawing FIG. 5 is tested in the substrate testing station 210. The designator 340 may be applied prior to entering the substrate testing station or while at such substrate testing station 210. Variations of designator 340 are disclosed in ~~Application No. 09/650,796,~~ U.S. Patent 6,415,977, also assigned to Micron Technology, Inc., which discloses a method and apparatus for marking and identifying a defective die site utilizing a designator within the contemplated scope of the designator 340 of the present invention, the disclosure of which is incorporated herein by this reference.

Please amend paragraph number **[0055]** as follows:

[0055] Preferably, the mapped information correlates with the test and inspection information with respect to individual semiconductor die sites and a particular substrate configuration can be used to create a computerized map of the substrate, the computerized substrate map comprising test and inspection data related to the functionality of each of the semiconductor die sites and stored in computer memory as electronic file 220. Data within the electronic file 220 may then be transferred electronically to and from various fabrication stations, as shown in drawing FIG. 4, for processing the semiconductor die packages. As such, the mapped information in electronic file 220 is used in combination with designator 340 having the bar code of the present invention.